IN THE CLAIMS:

Please amend claims 1-3, 5, 7, and 11, as shown in the complete list of claims that is presented below.

1. (currently amended) A digital filter circuit comprising:

a first RAM that ~~latches~~ stores sequentially input data [[each]] having a first sampling period and sequentially outputs the data stored in the first RAM;

a second RAM that ~~latches~~ stores sequentially input data [[each]] having a second sampling period sequentially outputs the data stored in the second RAM;

a first register that ~~latches~~ stores the data sequentially outputted from the first RAM sequentially outputs the data stored in the first register;

a second register that ~~latches~~ stores the data sequentially outputted from the second RAM and sequentially outputs the data stored in the second register;

a cumulative arithmetic unit that computes the data outputted from the first RAM and the second RAM; and

a selector that alternately outputs the data outputted from the first register and the second register to the cumulative arithmetic unit.

2. (currently amended) A digital filter circuit according to claim 1, ~~which has the function of causing~~ wherein the data having the first sampling frequency or the data having the second sampling frequency is caused to partly disappear by overwriting new data on the data within the first register or the second register.

3. (currently amended) A digital filter circuit according to claim 1, ~~which has the function of feeding back~~ wherein the data computed by the cumulative arithmetic unit is fed back to the first register or the second register.

4. (original) A digital filter circuit according to claim 1, wherein the selector is operated to mix the data outputted from the first register or the second register with data outputted from the other register.

5. (currently amended) A digital filter circuit according to claim 1, ~~which has the function of directly inputting~~ wherein the digital filter circuit also has a mode in which the data having the first sampling period is directly inputted to the first register without being ~~latched~~ stored in the first RAM.

6. (original) A digital filter circuit according to claim 1, wherein the cumulative arithmetic unit includes a multiplier and an adder that adds data outputted from the multiplier.

7. (currently amended) A data processing method comprising the steps of:

sequentially inputting ~~and latching~~ data [[each]] having a first sampling period to [[and in]] a first RAM and storing the data having the first sampling period in the first RAM;

sequentially inputting ~~and latching~~ data [[each]] having a second sampling period to [[and in]] a second RAM and storing the data having the second sampling period in the second RAM;

sequentially outputting ~~and latching the~~ data sent from the first RAM to [[and in]] a first register and storing data sent from the first RAM in the first register;

sequentially outputting ~~and latching the~~ data sent from the second RAM to [[and in]] a second register and storing the data sent from the second RAM in the second register;

alternately outputting [[the]] data from sent the first register and the second register to a cumulative arithmetic unit; and

computing the data outputted to the cumulative arithmetic unit.

8. (original) A data processing method according to claim 7, further comprising the step of causing the data having the first sampling frequency or the data having the second sampling frequency to partly disappear by overwriting new data on the data within the first register or the second register.

9. (original) A data processing method according to claim 7, further comprising the step of feeding back the data computed by the cumulative arithmetic unit to the first register or the second register.

10. (original) A data processing method according to claim 7, further comprising the step of mixing the data outputted from the first register or the second register with data outputted from the other register.

11. (currently amended) A data processing method according to claim 7, ~~further comprising the step of directly inputting~~ wherein the method includes a mode in which the data having the first sampling period in input directly to the first register without being ~~latched~~ stored in the first RAM.

12. (original) A data processing method according to claim 7, wherein the cumulative arithmetic unit includes a multiplier and an adder that adds data outputted from the multiplier.